Amendments to the Claims

1-2. (Cancelled)

3. (Currently Amended) The method according to claim [[2]] 4, wherein ~~the step of measuring a time~~ the step of determining the data transfer speed includes measuring a time required to store a predetermined number of bits of the encoded data signal in the memory by counting pulses of a reference clock signal ~~to measure the time~~.

4. (Original) A method of transferring an encoded data signal including a clock signal and a data signal, comprising the steps of:

decoding the encoded data signal to generate a decoded data signal and a write clock signal;

storing the decoded data signal in a memory in accordance with the write clock signal;

determining a transfer speed of the encoded data signal using the write clock signal;

generating a read clock signal having a frequency corresponding to the determined data transfer speed;

reading the decoded data signal stored in the memory in accordance with the read clock signal; and

encoding the read decoded data signal and the read clock signal to generate an encoded data signal.

5. (Original) The method according to claim 4, wherein the step of determining the data transfer speed includes the steps of:

measuring a time required to store a predetermined number of bits of the encoded data signal in the memory; and

determining the data transfer speed based on the measured time.

6. (Original) The method of according to claim 5, wherein the step of measuring a time includes counting pulses of a reference clock signal to measure the time.

7. (Original) The method according to claim 6, wherein the step of generating the read clock signal includes the steps of:

generating a plurality of read clock signals corresponding to a plurality of data transfer speeds using the reference clock signal; and

selecting a read clock signal corresponding to a determined data transfer speed from the plurality of read clock signals.

8. (Original) The method according to claim 4, wherein the encoded signal includes a strobe signal and a data signal, which are encoded in accordance with a Data-Strobe Link coding scheme.

9. (Original) An apparatus for transferring an encoded data signal including a clock signal and a data signal, comprising:

an decoder circuit for decoding the encoded data signal to generate a decoded data signal and write clock signal;

a memory, connected to the decoder circuit, for storing the decoded data signal in accordance with the write clock signal;

a transfer speed determining circuit for determining a transfer speed of the encoded data signal in accordance with the write clock signal, wherein the transfer speed determining circuit generates a read clock signal having a frequency corresponding to the determined transfer speed, and the decoded data signal is read from the memory in accordance with the read clock signal; and

an encoder circuit, connected to the memory and the transfer speed determining circuit, for encoding the decoded data signal and the read clock signal to generate the encoded data signal.

10. (Original) The apparatus according to claim 9, wherein the memory includes:

a memory cell circuit for storing the decoded data signal;

a write pointer, connected to the memory cell circuit, for generating a write address of the memory cell circuit in accordance with the write clock signal;

a read pointer, connected to the memory cell circuit, for generating a read address of the memory cell circuit in accordance with the read clock signal; and

a pointer comparator, connected to the write pointer and the read pointer, for comparing the write address with the read address to generate a comparison result signal, and wherein the transfer speed determining circuit includes:

a timer, connected to the pointer comparator, responsive to the comparison result signal to measure a time required to store a predetermined number of bits of the decoded signal in the memory cell circuit in accordance with the write clock signal;

a determining circuit, connected to the timer, for determining the transfer speed based on the time measured by the timer to generate a determination signal; and

a clock signal generator circuit, connected to the determining circuit, for generating a read clock signal having a frequency corresponding to the determined transfer speed in accordance with the determination signal.

11. (Original) The apparatus according to claim 10, wherein the timer counts pulses of a reference clock signal in response to the comparison result signal while the predetermined number of bits of the decoded data signal are stored in the memory cell circuit in accordance with the write clock signal.

12. (Original) The apparatus according to claim 10, wherein the clock signal generator circuit generates a plurality of read clock signals corresponding to a plurality of data transfer speeds using the reference clock signal and selects a read clock signal corresponding to the determined data transfer speed from the plurality of read clock signals in accordance with the determination signal.